C1 Cont

dynamically enabling a second tristate driver having third and fourth driver transistors, an input coupled to a second logic element and an output directly connected to the interconnect line, such that a second signal is driven from the second logic element onto the interconnect line using the second tristate driver.

34. (previously added) The method of claim 33 further comprising: dynamically tristating the second tristate driver.

35. (previously added) The method of claim 33 wherein the first tristate driver is dynamically tristated without reconfiguring a memory cell.

36. (previously added) The method of claim 35 wherein the second tristate driver is dynamically enabled without reconfiguring a memory cell.

37. (previously added) The method of claim 33 wherein the first tristate driver is dynamically tristated using a first tristate control circuit.

38. (previously added) The method of claim 37 wherein the second tristate driver is dynamically enabled using a second tristate control circuit.

39. (previously added) The method of claim 33 wherein the first tristate driver is dynamically tristated using a third logic element.

40. (previously added) The method of claim 39 wherein the second tristate driver is dynamically enabled using a fourth logic element.

Claims 41-47 (previously canceled)

C2

48. (currently amended) A programmable logic integrated circuit comprising:

a first programmable interconnect bus;

a first plurality of logic elements configurable to perform logical functions;

C2 cont'd

a plurality of tristate devices coupled between the first plurality of logic elements and the first programmable interconnect bus;

a dedicated tristate device having an input coupled to the first programmable interconnect bus;

a second programmable interconnect bus coupled to an output of the dedicated tristate device;

a second plurality of logic elements configurable to perform logical functions and coupled to the second programmable interconnect bus;

a plurality of programmable memory cells coupled to the plurality of tristate devices to programmably enable and programmably tristate the plurality of tristate devices; and

tristate control logic having outputs coupled only to the plurality of tristate devices to dynamically enable and dynamically tristate the plurality of tristate devices.

49. (previously added) The integrated circuit of claim 48 wherein the tristate control logic is programmably coupled to signals on the programmable interconnect bus for controlling the states of the plurality of tristate devices.

50. (previously added) The integrated circuit of claim 48 wherein one of the plurality of logic elements is coupled through one of the plurality of tristate devices through the programmable interconnect bus to another one of the plurality of logic elements.

51. (previously added) The integrated circuit of claim 48 wherein the tristate control logic comprises a logic element.

C3

52. (currently amended) A programmable logic integrated circuit comprising:

a first logic element having a first output;

C3 cont'd

a first tristate driver having a first enable input, a second enable input, a second output, and a first input coupled to the first output;

a first programmable memory cell coupled to the first enable input;

a second logic element coupled to the second enable input;

a third logic element having a third output;

a second tristate driver having a third enable input, a fourth output, and a second input coupled to the third output;

a second programmable memory cell coupled to the third enable input; and

an interconnect line coupled to the second output and the fourth output,

wherein the interconnect line is not coupled to the second input and the fourth input by a programmable connection, and the second logic element may dynamically tristate and dynamically enable the first tristate driver.

53. (previously added) The integrated circuit of claim 52 wherein the interconnect line is a vertical conductor.

54. (previously added) The integrated circuit of claim 52 wherein the interconnect line is in a tristate bus.

55. (previously added) The method of claim 33 wherein the first tristate driver is dynamically tristated without writing to a memory cell.

56. (currently amended) An integrated circuit comprising:

C4

a first logic element having an output;

a first tristate driver having an input coupled to the output of the first logic element, and an output;

a second logic element having an output;

a second tristate driver having an input coupled to the output of the second logic element, and an output; [**and**]

C4 cont

[an] a first interconnect **[line]** bus coupled to the output of the first tristate driver and coupled to the output of the second tristate driver**[,]** ;

a second interconnect bus;

a third tristate driver having an input coupled to the first interconnect bus and an output coupled to the second interconnect bus;

third and fourth logic elements having inputs coupled to the second interconnect bus,

wherein **[the output of the first tristate driver is not coupled by a programmable connection to the interconnect line, the output of the second tristate driver is not coupled by a programmable connection to the interconnect line, and]** the first tristate driver, **[and]** the second tristate driver, and the third tristate driver **[may be]** are dynamically tristated and enabled.

57. (previously added) The integrated circuit of claim 56 wherein the first tristate driver is dynamically tristated without writing to a memory cell.

C5

58. (currently amended) An integrated circuit comprising:

a first tristate driver coupled between a first logic element and a first interconnect line;

an output enable generation circuit coupled to the first interconnect line; and

a second tristate driver coupled between a second logic element and a second interconnect line, wherein a control input of the second tristate driver is coupled to the output enable generation circuit. **[and**

a tristate control block having outputs coupled only to enable inputs of a plurality of tristate drivers,

wherein the plurality of tristate drivers comprises the first tristate driver and the second tristate driver.]

59. (canceled)

60. (previously added) The integrated circuit of claim 59 wherein the first tristate driver and the second tristate driver may be dynamically tristated and enabled.

61. (previously added) The integrated circuit of claim 60 wherein the first tristate driver and the second tristate driver are dynamically tristated without writing to a memory cell.